

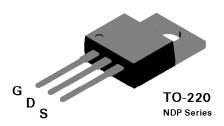
## NDP6060 / NDB6060 N-Channel Enhancement Mode Field Effect Transistor

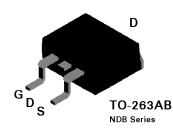
### **General Description**

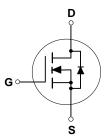
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

#### **Features**

- 48A, 60V.  $R_{DS(ON)} = 0.025\Omega$  @  $V_{GS} = 10V$ .
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R<sub>DS(ON)</sub>.
- TO-220 and TO-263 (D<sup>2</sup>PAK) package for both through hole and surface mount applications.







## Absolute Maximum Ratings

T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	NDP6060	NDB6060	Units		
V <sub>DSS</sub>	Drain-Source Voltage	60				
$V_{DGR}$	Drain-Gate Voltage ( $R_{GS} \le 1 \text{ M}\Omega$ )	60				
V <sub>GSS</sub>	Gate-Source Voltage - Continuous	±20				
	- Nonrepetitive (t <sub>p</sub> < 50 μs)	± 40				
I <sub>D</sub>	Drain Current - Continuous T <sub>c</sub> =25°C	48				
	- Continuous T <sub>c</sub> =100°C	32 144				
	- Pulsed					
P <sub>D</sub>	Total Power Dissipation @ T <sub>c</sub> = 25°C	10	00	W		
	Derate above 25°C	0.	W/°C			
$T_J$ , $T_{STG}$	Operating and Storage Temperature Range	-65 to 175				
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	2	75	°C		

Symbol	Parameter	Conditions			Тур	Max	Units
DRAIN-SC	DURCE AVALANCHE RATINGS (Note 1)						
W <sub>DSS</sub>	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25 \text{ V}, I_{D} = 48 \text{ A}$				200	mJ
I <sub>AR</sub>	Maximum Drain-Source Avalanche Cur	rent			48	Α	
OFF CHA	RACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	60			V	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$				250	μΑ
			T <sub>J</sub> = 125°C			1	mA
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	•			100	nA
GSSR	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHAR	RACTERISTICS (Note 1)						
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		2	2.9	4	V
			T <sub>J</sub> = 125°C	1.4	2.3	3.6	
$R_{\scriptscriptstyle DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_{D} = 24 \text{ A}$	·		0.02	0.025	Ω
				0.032	0.04		
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 10 \text{ V}$		48			Α
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 24 \text{ A}$		10	19		S
DYNAMIC	CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25 \text{ V}, \ V_{GS} = 0 \text{ V},$			1190	1800	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz			475	800	pF
C <sub>rss</sub>	Reverse Transfer Capacitance				150	400	pF
SWITCHII	NG CHARACTERISTICS (Note 1)						
t <sub>D(on)</sub>	Turn - On Delay Time	$V_{DD} = 30 \text{ V}, I_{D} = 48 \text{ A},$		10	20	nS	
ţ	Tum - On Rise Time	$V_{GS}$ = 10 V, $R_{GEN}$ = 7.5 $\Omega$		145	300	nS	
t <sub>D(off)</sub>	Turn - Off Delay Time	1			28	60	nS
ţ,	Turn - Off Fall Time				77	150	nS
$Q_g$	Total Gate Charge	$V_{DS} = 48 \text{ V},$			39	70	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS} = 48 \text{ V},$ $I_{D} = 48 \text{ A}, V_{GS} = 10 \text{ V}$			7.6		nC
$Q_{gd}$	Gate-Drain Charge				22		nC

Symbol	Parameter	Conditions	Conditions				Units
DRAIN-S	OURCE DIODE CHARACTERISTICS	•					
l <sub>s</sub>	Maximum Continuos Drain-Source Diode				48	Α	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Fo			144	Α		
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 24 \text{ A (Note 1)}$			0.9	1.3	V
			T <sub>J</sub> = 125°C		8.0	1.2	•
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_F = 48 \text{ A},$		35	87	140	ns
I <sub>rr</sub>	Reverse Recovery Current	$dl_{F}/dt = 100 \text{ A/}\mu\text{s}$		2	3.6	8	Α
THERMA	L CHARACTERISTICS	<u>.</u>				•	
R <sub>øJC</sub>	Thermal Resistance, Junction-to-Case			1.5	°C/W		
R <sub>eJA</sub>	Thermal Resistance, Junction-to-Ambier			62.5	°C/W		

Note: 1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

## **Typical Electrical Characteristics**

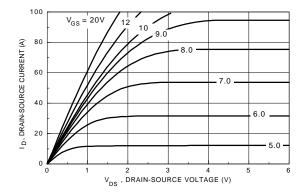


Figure 1. On-Region Characteristics

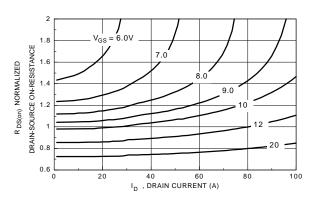


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

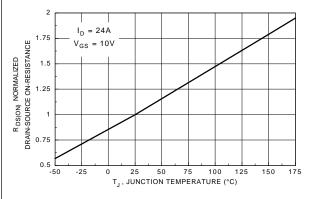


Figure 3. On-Resistance Variation with Temperature

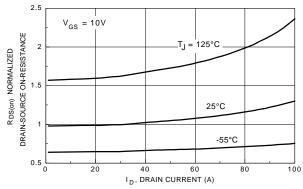


Figure 4. On-Resistance Variation with Drain Current and Temperature

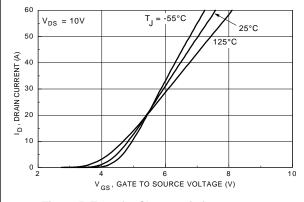


Figure 5. Transfer Characteristics

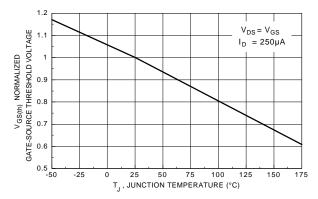


Figure 6. Gate Threshold Variation with Temperature

## **Typical Electrical Characteristics (continued)**

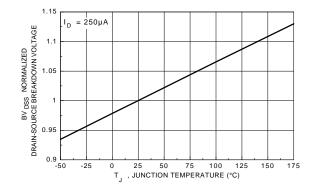


Figure 7. Breakdown Voltage Variation with Temperature

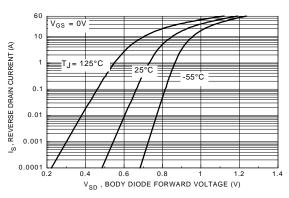


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

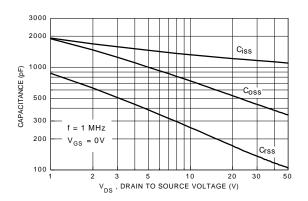


Figure 9. Capacitance Characteristics

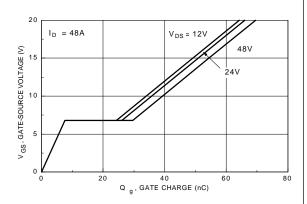


Figure 10. Gate Charge Characteristics

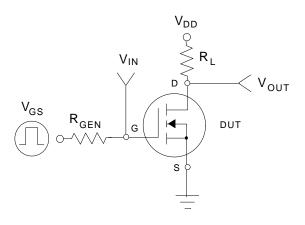


Figure 11. Switching Test Circuit

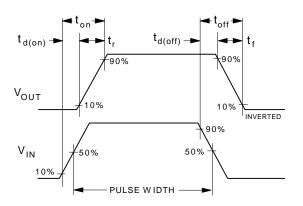
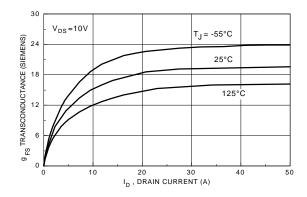


Figure 12. Switching Waveforms

## **Typical Electrical Characteristics (continued)**



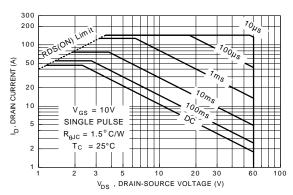


Figure 13. Transconductance Variation with Drain Current and Temperature

Figure 14. Maximum Safe Operating Area

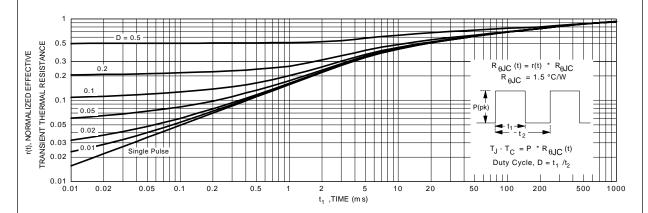
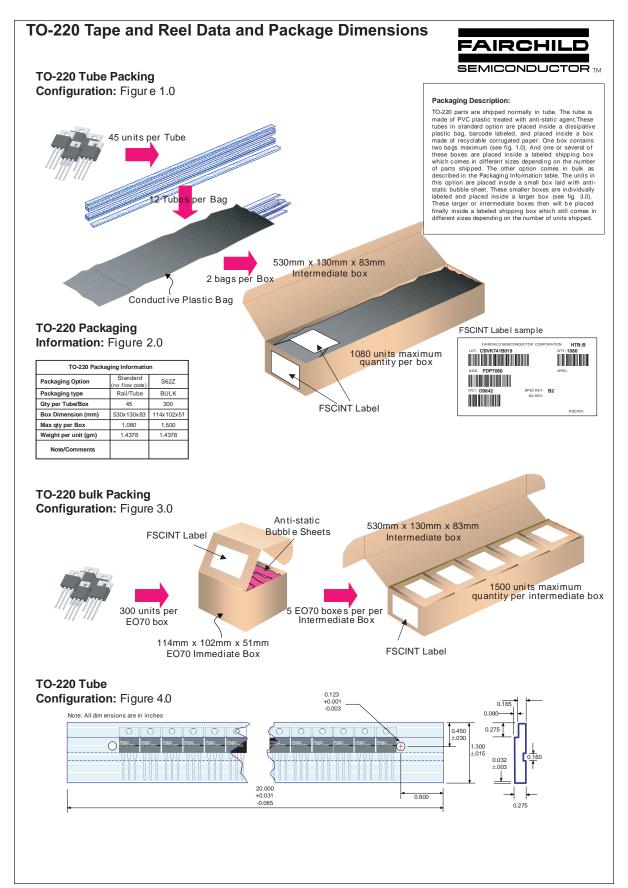
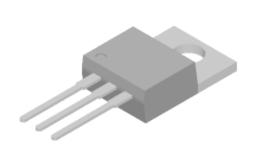


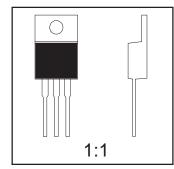
Figure 15. Transient Thermal Response Curve



## TO-220 Tape and Reel Data and Package Dimensions, continued

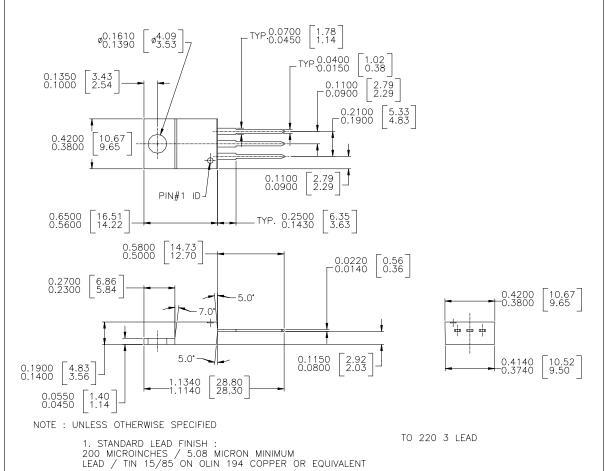
# TO-220 (FS PKG Code 37)

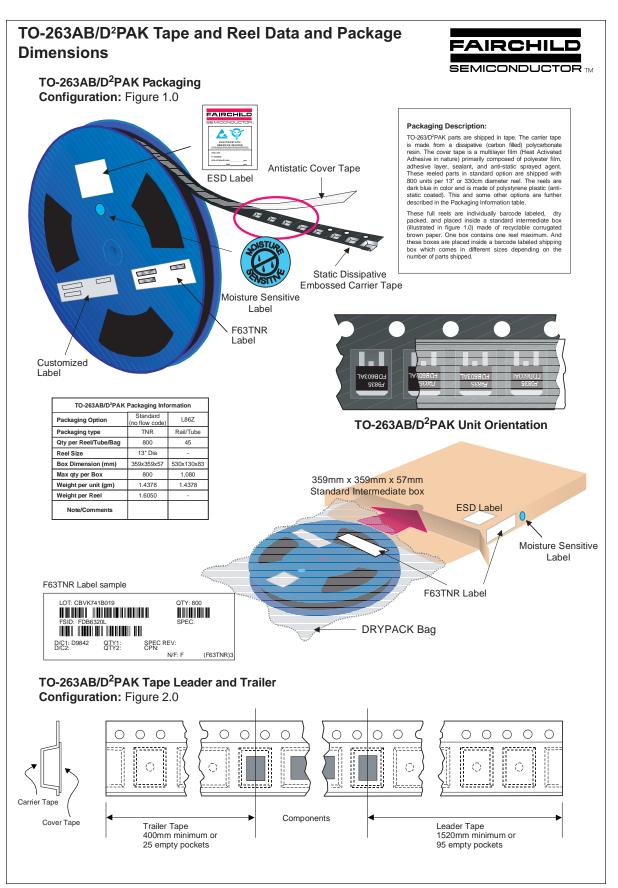




Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

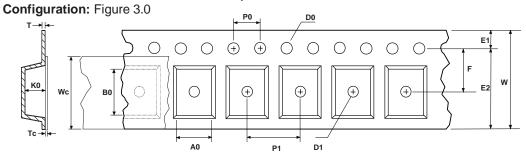
Part Weight per unit (gram): 1.4378





# TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued

## TO-263AB/D<sup>2</sup>PAK Embossed Carrier Tape



# User Direction of Feed

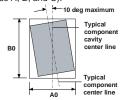
Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
TO263AB/ D <sup>2</sup> PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)

Component Rotation

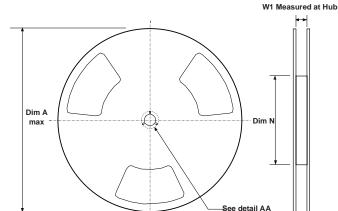


Sketch B (Top View)
Component Rotation

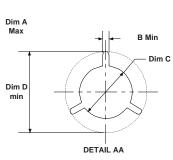


Sketch C (Top View)
Component lateral movement

# **TO-263AB/D<sup>2</sup>PAK Reel Configuration:** Figure 4.0



13" Diameter Option

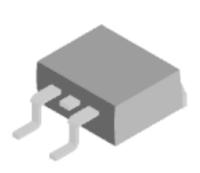


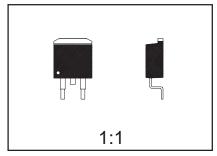
W2 max Measured at Hub

Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
24mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.961 +0.078/-0.000 24.4 +2/0	1.197 30.4	0.941 - 0.1.079 23.9 - 27.4

## TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued

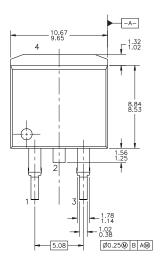
# TO-263AB/D<sup>2</sup>PAK (FS PKG Code 45)

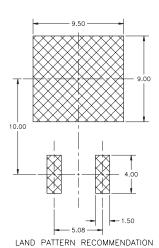


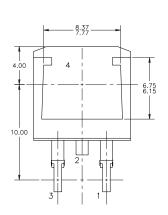


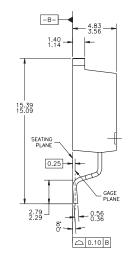
Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 1.4378









- NOTES: UNLESS OTHERWISE SPECIFIED

  A) ALL DIMENSIONS ARE IN MILLIMETERS.
  B) STANDARD LEAD FINISH:
  200 MICROINCHES / 5.08 MICROMETERS MIN.
  LEAD/TIN 15/85 ON OLIN 194 COPPER OR
  EQUIVALENT.
  C) MAXIMUM YERTICAL BURR ON HEATSINK NOT
  TO EXCEED 0.003 INCH / 0.05mm.
  D) NO PACKAGE CHIPS, CRACKS OR SURFACE
  IDENTIFICATION ALLOWED AFTER FORMING.
  E) REFERENCE JEDEC, TO—265, ISSUE C,
  VARIATION AB, DATED 2/92.

### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

FACT $^{\text{TM}}$  QFET $^{\text{TM}}$  FACT Quiet Series $^{\text{TM}}$  QS $^{\text{TM}}$ 

 $\begin{array}{lll} \mathsf{FAST}^{\circledast} & \mathsf{Quiet}\,\mathsf{Series^{\mathsf{TM}}} \\ \mathsf{FASTr^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}\text{-}3} \\ \mathsf{GTO^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}\text{-}6} \\ \mathsf{HiSeC^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}\text{-}8} \\ \end{array}$ 

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### PRODUCT STATUS DEFINITIONS

### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.